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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/699,890

11/04/2003

Takashi Terauchi

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3485

22850

7590

06/22/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
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ALEXANDRIA, VA 22314

EXAMINER

TRAN, MAI HUONG C

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,890	TERAUCHI ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 1-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/4/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group I (claims 12-17) drawn to a semiconductor device is acknowledged. Accordingly, claims 1-11 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentability of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,744,091 to Ema et al. in view of Mizutani et al. (6,433,381).

Regarding to claims 12-14, Ema et al. discloses a semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with the data holding portion, the data holding portion and the peripheral circuit portion being formed on a same semiconductor substrate, the semiconductor device comprising gate interconnections 20, 22 provided respectively in the data holding portion and the peripheral circuit portion on the semiconductor substrate 10, each gate interconnection having its top covered by a silicon nitride film 18; first sidewall nitride films 30 provided respectively on sides of the gate interconnections in the data holding portion and the peripheral circuit portion; first and second impurity regions provided in the data holding portion and the peripheral circuit portion, respective first and second impurity regions being selectively formed in the surface of the semiconductor substrate

that extend outward from sides of the respective gate interconnections (col. 11, lines 43-49); sidewall insulating films (col. 11, lines 49-56) provided on sides of the first sidewall nitride films of the gate interconnection in the peripheral circuit portion; contact plugs 44 composed of a conductive silicon and passing through a first interlayer insulating film provided on the data holding portion to reach the surface of the semiconductor substrate where the first and second impurity regions are formed; and metal silicide films (col. 39, lines 46-50) provided on all contact plugs in the data holding portion and on the surface of the semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed (col. 24, lines 19-67, col. 25, and figs 1-2).

Ema et al. do not disclose third impurity regions provided in the peripheral circuit portion, the third impurity regions being selectively formed in the surface of the semiconductor substrate that extend outward from sides of the sidewall insulating films and having a higher impurity concentration than the first and second impurity regions.

Mizutani et al. teach third impurity regions provided in the peripheral circuit portion as set forth in col. 24, lines 57-62.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form third impurity regions provided in the peripheral circuit portion, as taught by Mizutani in order to provide a semiconductor device capable of increasing the pattern precision of the bit lines and the wirings which have a different film thickness, and reducing resistances of the bit lines and the wirings by forming shallow through holes that are formed between the bit lines in the self-alignment manner,

and also improving lower resistance and throughput of the bit lines and the wirings (col. 7, lines 14-21).

Regarding to claims 15-17, Ema et al. discloses a semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with the data holding portion, the data holding portion and the peripheral circuit portion being formed on a same semiconductor substrate, the semiconductor device comprising gate interconnections 20, 22 provided respectively in the data holding portion and the peripheral circuit portion on the semiconductor substrate 10, each gate interconnection having its top covered by a silicon nitride film 18; first sidewall nitride films 30 provided respectively on sides of the gate interconnections in the data holding portion and the peripheral circuit portion; first and second impurity regions provided in the data holding portion and the peripheral circuit portion, respective first and second impurity regions being selectively formed in the surface of the semiconductor substrate that extend outward from sides of the respective gate interconnections (col. 11, lines 43-49); sidewall insulating films (col. 11, lines 49-56) provided on sides of the first sidewall nitride films of the gate interconnection in the peripheral circuit portion; contact plugs 44 composed of a conductive silicon and passing through a first interlayer insulating film provided on the data holding portion to reach the surface of the semiconductor substrate where the first and second impurity regions are formed; and a metal silicide films (col.

39, lines 46-50) provided only on the surface of the semiconductor substrate in the peripheral circuit portion where the third impurity regions are formed (col. 24, lines 19-67, col. 25, and figs 1-2).

Ema et al. do not disclose third impurity regions provided in the peripheral circuit portion, the third impurity regions being selectively formed in the surface of the semiconductor substrate that extend outward from sides of the sidewall insulating films and having a higher impurity concentration than the first and second impurity regions.


Mizutani et al. teach third impurity regions provided in the peripheral circuit portion as set forth in col. 24, lines 57-62.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form third impurity regions provided in the peripheral circuit portion, as taught by Mizutani in order to provide a semiconductor device capable of increasing the pattern precision of the bit lines and the wirings which have a different film thickness, and reducing resistances of the bit lines and the wirings by forming shallow through holes that are formed between the bit lines in the self-alignment manner, and also improving lower resistance and throughput of the bit lines and the wirings (col. 7, lines 14-21).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Mai-Huong Tran


David Nelms
Supervisory Patent Examiner
Technology Center 2800